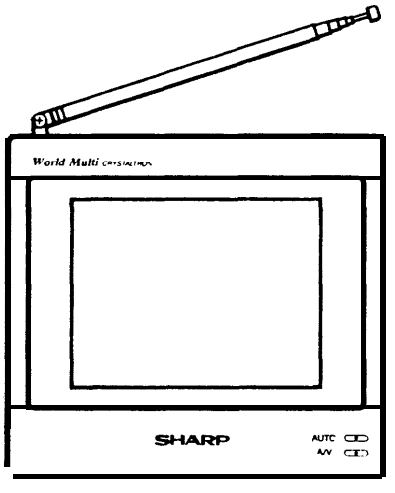
SHARP TECHNICAL MANUAL

LCD COLOUR TELEVISION
MODEL 6M-10G/S



CONTENTS

SHARP CORPORATION

1. TUNING VOLTAGE GENERATING & AUDIO MUTE CIRCUITS

RH-iX1605CEZZ (TSC: Tuning System Control)

Outline

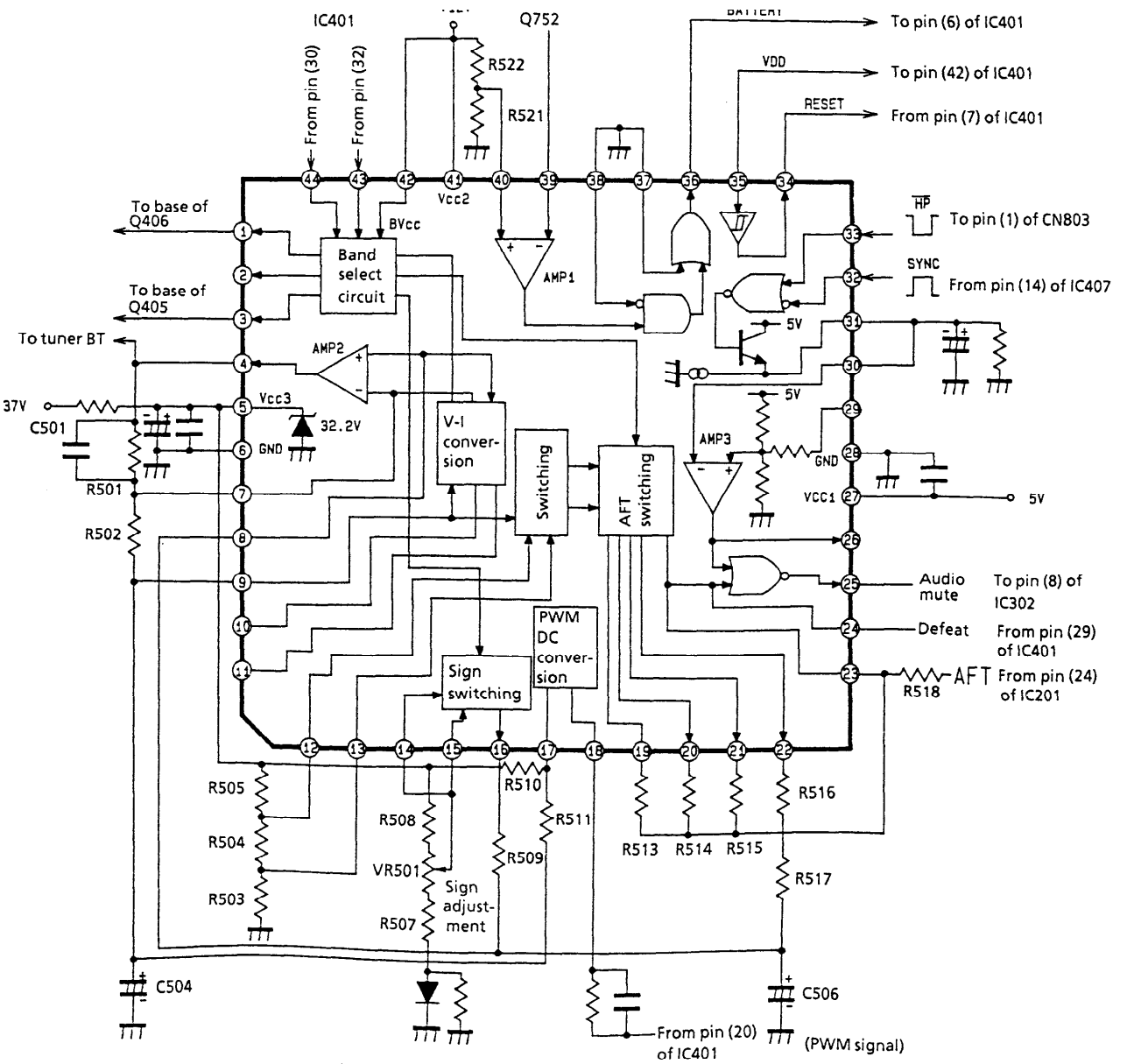
The iX1605CE is a multi-function integrated circuit designed for the **tuning** system of a voltage synthesizer type small colour TV set.

The functions of this IC include tuning voltage generation, AFT defeat and U/V switching, low voltage detection, U/V sign positioning, tuner band selection, reception **judgment,** audio muting, and resetting.

Features

1. Tuning voltage generating circuit
   - AFT defeat and U/V switching circuit
   - U/V sign positioning circuit
2. Tuner band selection circuit
3. Low voltage detection circuit
4. Reception judgment and audio mute circuit
5. Reset circuit

Basic connections



Circuit operation

(1) Pin functions

Pin No.	Name of terminal	Function	Pin No.	Name of terminal	Function
1	BO1	VHF band select output	23	AF-IN	AFT voltage input
2	BO2	UHF band select output	24	DEFEAT	Defeat signal input (positive polarity)
3	BO3	VHF-L/H select output	25	MUTE	Audio mute output
4	VT-OUT	Tuning voltage output	26	SYNC-OUT	Reception judgment output
5	VCC3	33V regulated power input	27	VCC1	+ 5V power input
6	GND	Grounding terminal	28	GND	Grounding terminal
7	VT-	Tuning voltage operational amplifier negative input	29	SYNC +	Reception judgment threshold preset
8	VT+	Tuning voltage operational amplifier positive input	30	SYNC-	Reception judgment
9	V-i	V-i conversion input	31	LPF	Capacitor connection for reception judgment low-pass filter
10	GAIN ADJ.	VHF tuning voltage gain adjusting resistor connection	32	SYNC	Sync signal input (positive polarity)
11	GAIN ADJ.	VHF tuning voltage gain adjusting resistor connection	33	$\overline{H.P}$	Horizontal pulse signal input (negative polarity)
12	TH1	AF1 output preset voltage	34	RESET OUT	Reset output
13	TH2	AF2 output preset voltage	35	VCC4	Reset power input (+ 5V)
14	UHF ADJ.	UHF sign output voltage control	36	LVF OUT	Low-voltage flag output
15	VHF ADJ.	VHF sign output voltage control	37	LVF IN	External voltage flag input
16	SIGN OUT	Sign output	38	Ni-Cd CTR	Ni-Cd identify control voltage input
17	PWM OUT	PWM amplifier output	39	NiCd-	Battery voltage input
18	PWM IN	PWM input	40	NiCd +	Low-voltage judgment preset voltage
19	AF1	AFT control voltage output	41	VCC2	+ 13V power input
20	AF2	AFT control voltage output	42	BVCC	BO3 power input (+ 13V)
21	AF3	UHF AFT control voltage output	43	B3	L/H band select input
22	AF OUT	AFT voltage output	44	B1	U/V band select input

Circuit behavior

(1) Tuning voltage generating circuit

PWM signal being inputted to pin (18) is amplified to 33V. The resulting signal is converted to a DC voltage by the low-pass filter that is composed of R510, R511 and C504. The DC voltage signal goes out of pin (9) through R502 into pin (7). The sign output voltage at pin (16) and the AFT output voltage at pin (22), on the other hand, are applied to R509 and R517, where these signals turn to be a composite signal. This signal is fed to pin (8) in order to control the tuning voltage. The AFT input voltage is fed through R518 and goes out of pin (22). Together with this AFT output voltage, pin (22) receives another output; that is a 1/2VCC1 voltage which is given out of pins (19), (20) and (21), and divided by R513, R514 and R515 respectively. Pin (21) stays in high impedance state at the selection of VHF, but gives out the 1/2VCC1 output at the selection of UHF. The AFT output voltage is then reduced, according to the ratio of R518 to R515, for switching between UHF and VHF. Pins (19) and (20) remain in high impedance state while the voltage at pin (9) is higher than the TH2 voltage at pin (13). With the voltage level somewhere between TH1 and TH2, pin (20) receives the 1/2VCC voltage and pin (19) is kept in high impedance state. When the voltage at pin (9) goes above the TH1 level, the 1/2VCC1 voltage is given into pins (19) and (20).

Table I

Input		output			
B1	V-I (V9)	AF1	AF2	AF3	VT OUT
L	*	—	—	ZH	—
H	*	—	—	1/2VCC1	—
*	V9>TH1	1/2VCC1	1/2VCC1	—	LOW
*	TH1 >V9>TH2	ZH	1/2VCC1	—	MIDDLE
*	TH2>V9	ZH	ZH	—	HIGH

TH1 = Voltage at pin (I 2) TH2 = Voltage at pin (13) ZH = High impedance
* = Don't care

(2) Tuner band select circuit

Tuner bands are selected by the input coming from the microcomputer IC401.

Table 2

Input		output		
B1	B3	BO1	BO2	BO3
L	L	VCC1	L	L
L	H	VCC1	L	BVCC
H	*	L	VCC1	ZH

* = Don't care ZH = High impedance BVCC = Voltage at pin (42)

(3) Low-voltage detection circuit

An output is fed to the microcomputer IC401 when the battery voltage has dropped. By this, the batterv indicator is activated.

Table 3

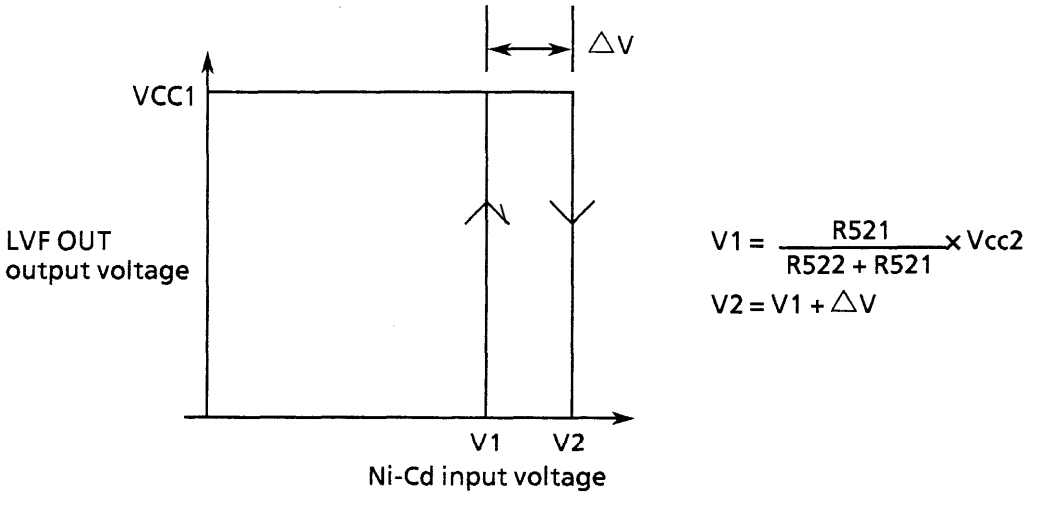
Input			output
LVF-IN	Ni-Cd control	NiCd-	LVF OUT
L	L	NiCd + < NiCd-	L (Note 1)
L	L	NiCd + < NiCd-	H (Note 1)
L	H or open	*	L
H or open	L	*	H
H or open	H or open	*	H

* = Don't care

Note 1: Hysteresis voltage △V

$$\triangle V = \frac{R522 \times R521}{R522 + R521} \times 25 \times 10^{-6}[V]$$

Figure. 1 Input/output characteristics



$$V1 = \frac{R521}{R522 + R521} \times Vcc2$$

$$V2 = V1 + \triangle V$$

(4) Reception judgment and audio mute circuit
The $\overline{HP}$ and the SYNC signals are compared with each other to mute the audio circuit if noises are received.

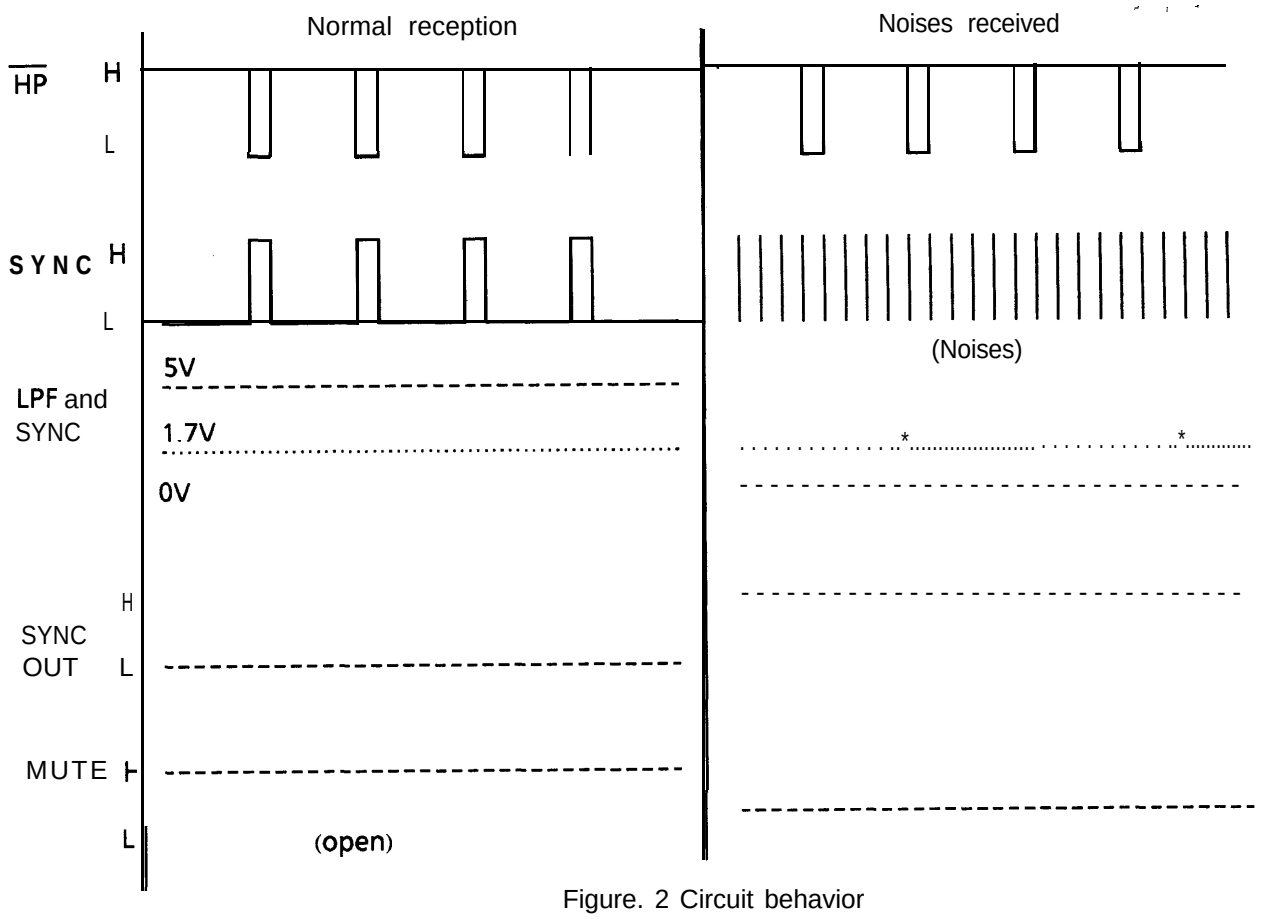


Figure. 2 Circuit behavior

(5) Reset circuit

The reset circuit is used for the microcomputer.
The VCC4 terminal is connected to the Vdd terminal of the microcomputer.

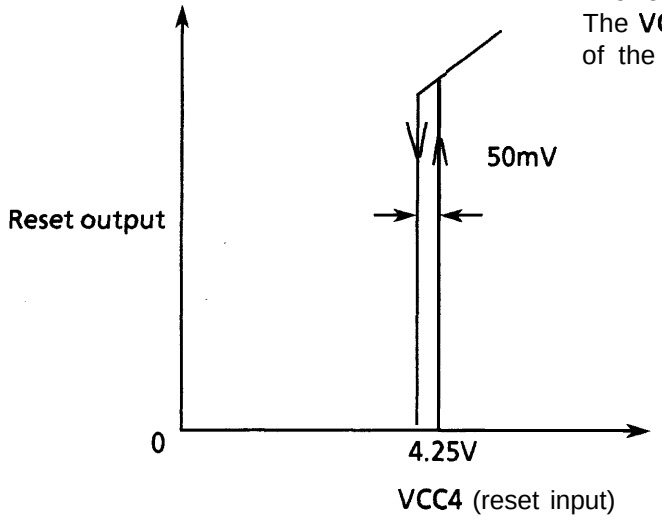


Figure. 3 Reset circuit input/output characteristics

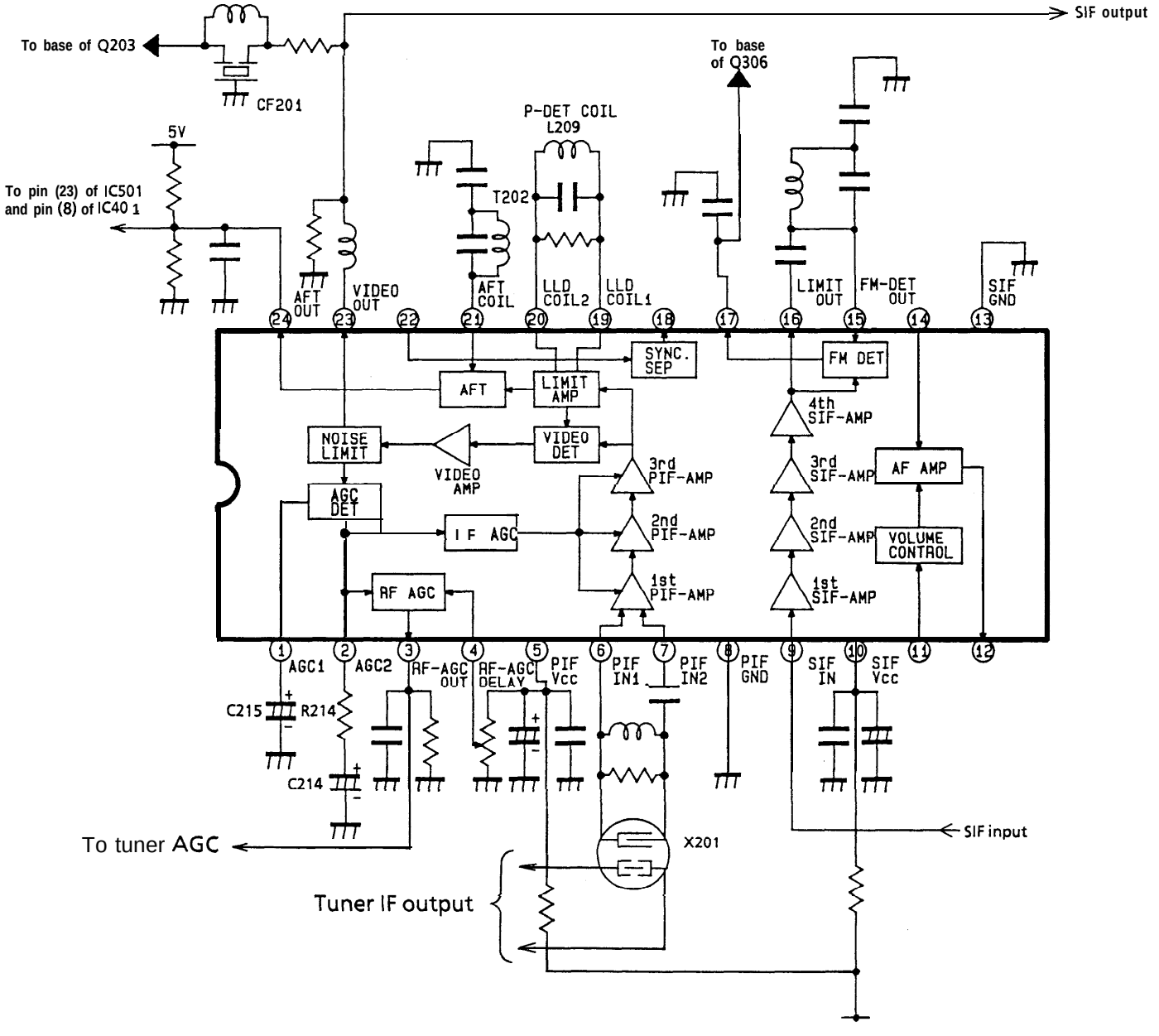
2. PIF/SIF CIRCUIT (TA8805F)

The PIF/SIF circuit is an IC for LCD television system. A double time constant circuit is composed of C215, R214 and C214 in order to improve the response time in automatic gain control.

Features

* Video IF amplification detector (LLP detector)
* Noise inverter
* IF AGC detector (with double time constant)
* RF AGC amplifier (forward AGC)
* AFT detector with MUTE function
* Audio IF amplification detector
* Electronic sound volume control
* Audio preamplifier (earphone direct-driven)

Basic connections



Pin functions

Pin No.	Name of terminal	Function
1	AGC1	Primary AGC filter terminal
2	AGC2	'Secondary AGC filter terminal
3	RF-AGC OUT	RF AGC control voltage output
4	RF-AGC DELAY	RE AGC delay adjustment terminal
5	PIF-VCC	PIF circuit power supply terminal
6	IF-IN1	IF signal input terminal
7	IF-IN2	IF signal input terminal
8	PIF-GND	PIF circuit grounding terminal
9	SIF IN	SIF signal input terminal
10	SIF VCC	SIF circuit power supply terminal
11	VOLUME CONT	Volume control terminal
12	AUDIO OUT	Audio output terminal
13	SIF GND	SIF circuit grounding terminal
14	AUDIO IN	Audio input terminal
15	FM DET IN	Audio FM detector input terminal
16	LIMIT OUT	SIF limiter output terminal
17	DE-EMP	Audio deemphasis terminal
18	SYNC. SEP	Sync separation signal output terminal
19	LLD COIL1	PIF detector carrier sampling terminal
20	LLD COIL2	PIF detector carrier sampling terminal
21	AFT COIL	AFT detector tuning coil terminal
22	SYNC. SEP IN	Sync separation signal input terminal
23	VIDEO OUT	Video detection output terminal
24	AFT OUT	AFT control voltage output terminal

CHROMA PROCESSING CIRCUIT (TA8795AF)

The TA8795AF integrated circuit is intended for processing the multi-input (in NTSC, SECAM and PAL systems) video and chroma signals and for sync separation.
The video signal is fed to pin (2), whereas the chroma signal is sent to pin (21) (for NTSC or PAL system) or pin (24) (for SECAM system). The video signal for sync separation goes into pin (13).
The video signal via pin (13) is first amplitude-separated in the sync separator and goes to the vertical integrating circuit to pick up the external vertical sync signal. The horizontal sync signal, on the other hand, goes through the AFC detection, 32fH oscillation and horizontal count-down circuits - - making a loop - - in order to get a horizontal pulse signal in sync with the external sync signal.
When the external vertical sync signal has a constant pulse width and period and flows continuously, this signal resets the vertical count-down circuit, thereby producing the vertical sync signal. If the external vertical sync signal does not meet the above conditions, the internal vertical sync signal is outputted to provide stable vertical sync even without any external sync signal.
The video signal via pin (2) is pedestal-clamped and fed through the following circuits for demodulation.

- Black stretching circuit
  This circuit is used to stretch below-the-level signals toward the black portion. Clear images can be achieved.
- DC transmission factor compensating circuit
  This circuit prevents white compression on a light screen and black compression on a dark screen.
- Sharpness enhancing circuit
- Dynamic gamma circuit
  This circuit too prevents white compression on a light screen.

The chroma signal is identified by the identification circuit and goes out of pins (31), (38) and (15). These pins double as manual mode input terminals. (See the table below.)
In the PAL and SECAM systems, the chroma signal goes out of pin (28) and into the 1H delay line. The 1H delay line output is fed to pin (30) for chroma signal processing. The resulting signal proceeds to the demodulation circuit.

Outputs in automatic mode

Signal received	Pin (31)	Pin (38)	Pin (15)
PAL	H	H	M
SECAM	H	M	M
4.43 NTSC	L	H	M
3.58 NTSC	L	L	M
Black-&-white	L	M/L	L

H : 3V
M : 1.5V
L : 0V

Inputs in manual mode

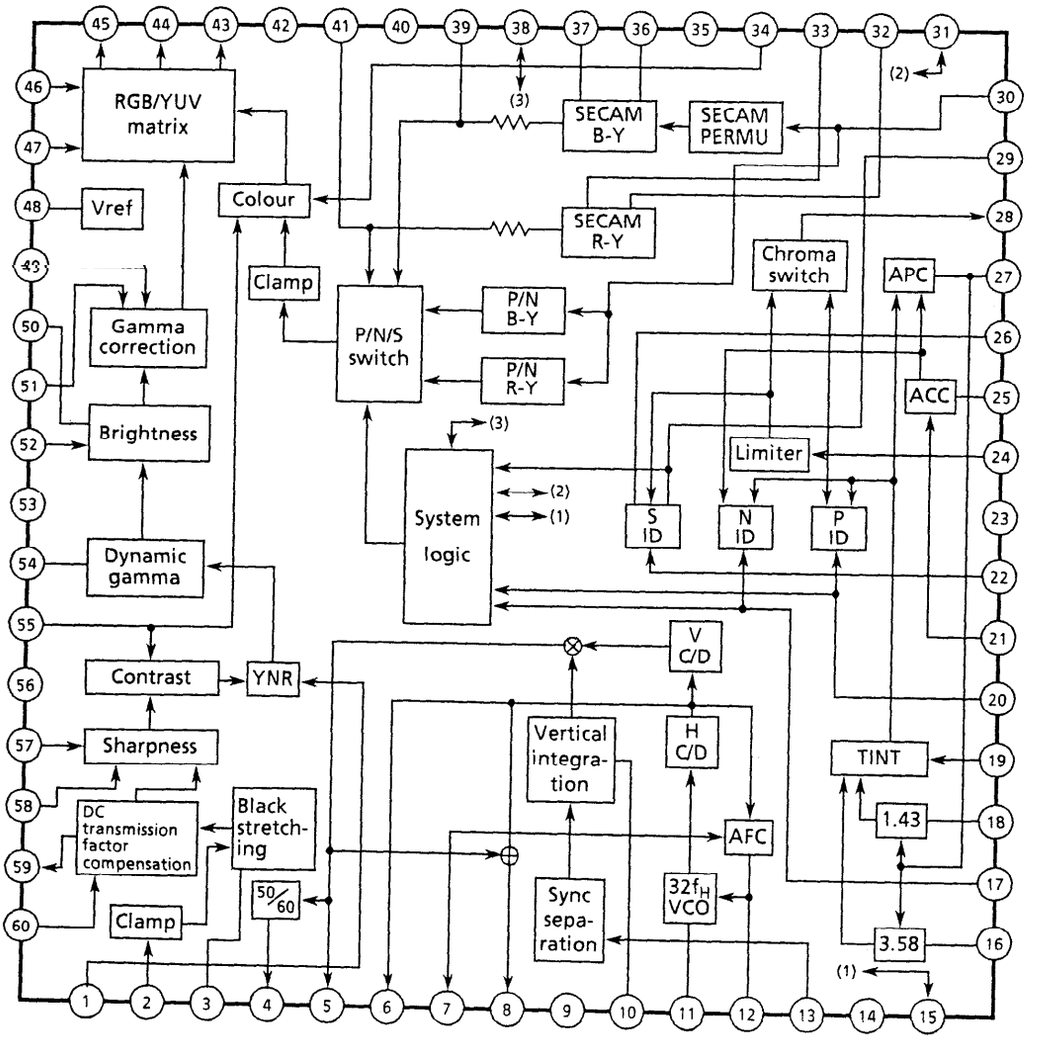
System	Pin (31)	Pin (38)	Pin (15)
PAL	H	H	H
SECAM	H	(M)	H
4.43 NTSC	(L)	H	H
3.58 NTSC	(L)	(L)	H

Levels in parentheses denote drive with high impedance.

Pin No.	Name of terminal	Function
1	NRSW	YNRswitch
2	YIN	Video signal input
3	Black PEAK	Time constant connection for black peak level
4	50/6OHz	Vertical sync identify output
5	VD OUT	Vertical output
6	HD OUT	Horizontal output
7	CP/SP	Clamp pulse/sync separation output
8	HD2	Horizontal sync output
9	Def GND	Ground for sync signal regenerative circuit
10	V INT	Vertical sync integrating capacitor
11	32Fh VCO	32f H resonator
12	AFC FILTER	Filter for automatic horizontal frequency control
13	SYNC IN	Video signal input for sync regeneration
14	Def Vcc	Sync signal regenerative circuit power
15	SW3	System logic input/output
16	3.58X	3.58MHz crystal oscillator connection
17	N-IDENT	NTSC identify filter connection
18	4.43x	4.43MHz crystal oscillator connection
19	TINT	Tint control connection
20	P-IDENT	PAL identify filter connection
21	P/N IN	PAL/NTSC chroma input
22	F-ID SW	SECAM identify switch
23	Chroma GND	Ground for chroma processing circuit
24	S IN	SECAM chroma input
25	ACC FILTER	ACC detection filter connection
26	SID Det	SECAM identify resonance coil connection
27	APC FILTER	APC filter connection
28	1H OUT	PAL/SECAM colour signal output of 1 H delay line
29	S ID	SECAM identify filter connection
30	1H IN	1 H delay line signal input of PAL/SECAM colour signal
31	SW1	System logic input/output
32	B-Y Del	SECAM detection tank coil connection
33	B-Y De2	SECAM detection tank coil connection
34	COLOUR	Colour control
35	c vcc	Chroma processing circuit power
36	R-Y Del	SECAM detection tank coil connection
37	R-Y De2	SECAM detection tank coil connection
38	SW2	System logic input/output
39	B-Y Dem	SECAM deemphasis filter connection
40		
41	R-Y Dem	SECAM deemphasis filter connection
42		
43	BOUT	Primary-colour (B) signal output
44	G OUT	Primary-colour (G) signal output

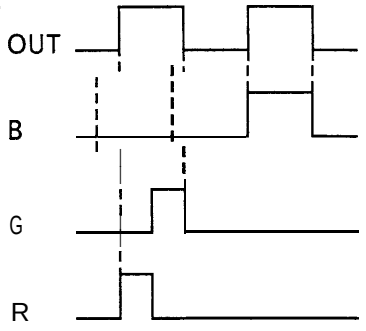
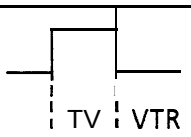
Pin No.	Name of terminal	Function
45	ROUT	Primary-colour (R) signal output
46	CLAMP FILTER	Clamp filter connection
47	PIP SW	Output signal mode selector
48	Vref	Reference voltage capacitor connection
49	γCONT2	Gamma correction control
50	Y CLAMP	Clamp capacitor connection
51	γCONT1	Gamma correction control
52	BRIGHT	Brightness control
53	Y-GND	Ground for video signal processing circuit
54	White PEAK	Time constant connection for white peak
55	CONTRAST	Contrast control
56	Y-Vcc	Video signal processing circuit power
57	PICTURE	Picture quality control
58	YH IN	Secondary differential signal input
59	APL IN	Black stretching
60	APL OUT	Black stretching

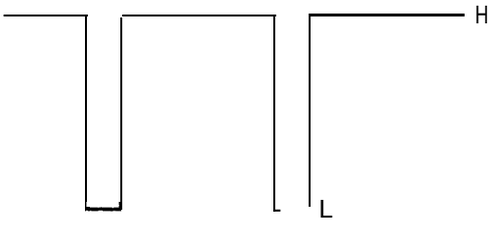
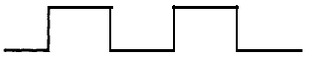
BLOCK DIAGRAM

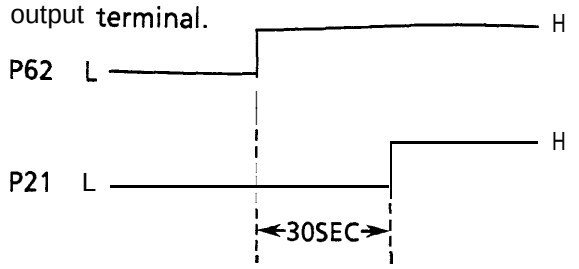


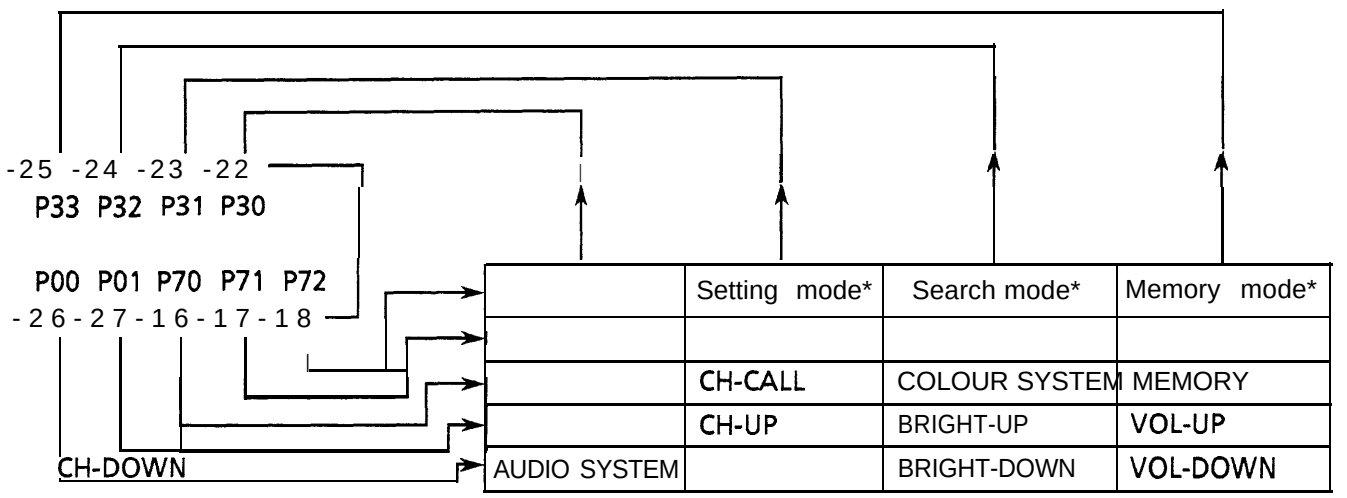
4. MICROCOMPUTERIZED CHANNEL SELECTOR CIRCUIT (M34300N4-740FP)

Discussed below are the functions and basic operation of this IC.

<table>
<tr><th>Pin No.</th><th>Name of terminal</th><th>I/O</th><th>Function/Terminal waveform</th></tr>
<tr><td>1
2
3
4</td><td>OUT
B
G
R</td><td>O
O
O
O</td><td>Blanking output for screen display (OR output).
BLUE output for sign display.
GREEN output for sign display.
RED output for sign display.
  </td></tr>
<tr><td>5</td><td>P4</td><td>I</td><td>TV/VTR mode signal input terminal.
  </td></tr>
<tr><td>6</td><td>P62</td><td>I</td><td>Battery alarm input “H”.</td></tr>
<tr><td>7</td><td>RESET</td><td>I</td><td>IC reset terminal. “H” in normal use.</td></tr>
<tr><td>8</td><td>P51</td><td>I</td><td>AFT voltage input terminal (/AD)</td></tr>
<tr><td>9</td><td>P50</td><td>I</td><td>“Hs” counter input. Composite sync signal is inputted.</td></tr>
<tr><td>10</td><td>VDP0</td><td>O</td><td>D/A output terminal for sound volume control.</td></tr>
<tr><td>11</td><td>VDP1</td><td>O</td><td>D/A output terminal for brightness control.</td></tr>
<tr><td>12
13</td><td>VDP2
VDP3</td><td>O
O</td><td>Audio system control signal generation
<table>
<tr><th>Audio system mode</th><th colspan="2">Colour system mode</th><th></th><th>VDP3</th><th>VDP2</th></tr>
<tr><td rowspan="6">AUTO</td><td rowspan="6">Forced AUTO</td><td>PAL, SECAM, N4.43</td><td></td><td>L</td><td>L</td></tr>
<tr><td>N3.58</td><td></td><td>H</td><td>H</td></tr>
<tr><td>PAL, SECAM, N4.43</td><td></td><td>L</td><td>L</td></tr>
<tr><td>N3.58</td><td></td><td>H</td><td>H</td></tr>
<tr><td rowspan="2">Black-&-white</td><td>50Hz</td><td>L</td><td>L</td></tr>
<tr><td>60Hz</td><td>H</td><td>H</td></tr>
<tr><td>Forced 1</td><td colspan="2"></td><td></td><td>L</td><td>H</td></tr>
<tr><td>Forced 2</td><td colspan="2"></td><td></td><td>L</td><td>L</td></tr>
<tr><td>Forced 3</td><td colspan="2"></td><td></td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>14</td><td>P53</td><td>I</td><td>50/60 Hz input select. L: 50 Hz, H: 60 Hz.</td></tr>
<tr><td>15</td><td>P60</td><td>O</td><td>Sync detect output terminal. Sync detection is made by counting the input pulses at P50. “H” when in sync.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Name of terminal</th><th>I/O</th><th>Function/Terminal waveform</th></tr>
<tr><td>16
17
18
26
27</td><td>P70
P71
P72
P00
P01</td><td>0
0
0
0
0</td><td>Key strobe output.
  </td></tr>
<tr><td>19</td><td>TEST</td><td>I</td><td>Connected to GND.</td></tr>
<tr><td>20</td><td>D/A</td><td>0</td><td>PWM output for tuning voltage.
  </td></tr>
<tr><td>21</td><td>GND</td><td></td><td>Grounding terminal.</td></tr>
<tr><td>22
23
24
25</td><td>P30
P31
P32
P33</td><td>I
I
I
I</td><td>Key matrix strobe input terminal.</td></tr>
<tr><td>28
31</td><td>P02
P11</td><td>0
0</td><td>Colour mode control output.
<table>
<tr><th></th><th>P02</th><th>P11</th></tr>
<tr><td>PAL</td><td>L</td><td>L</td></tr>
<tr><td>SECAM</td><td>L</td><td>H</td></tr>
<tr><td>N4.43</td><td>H</td><td>L</td></tr>
<tr><td>N3.58</td><td>H</td><td>H</td></tr>
<tr><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>29</td><td>P03</td><td>0</td><td>DEF output to turn off AFT.</td></tr>
<tr><td>30
32</td><td>P10
P12</td><td>0
0</td><td>Generation of tuner’s control (band) signal.
<table>
<tr><th></th><th>V_L</th><th>V_H</th><th>U</th></tr>
<tr><td>P10</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>P12</td><td>H</td><td>L</td><td>L</td></tr>
</table></td></tr>
<tr><td>33</td><td>P61</td><td>0</td><td>AUTO LED light-up output. Light-up at “L”.</td></tr>
<tr><td>34
35</td><td>Xin
Xout</td><td></td><td>System clock oscillation terminal (4 MHz).</td></tr>
<tr><td>36</td><td>P20</td><td>0</td><td>Colour mode control output. Auto at “H”, Forced at “L”.</td></tr>
</table>

Pin No.	Name of terminal	I/O	Function/Terminal waveform
37	P21	0	Fluorescent lamp control output terminal. 
38	VSYNC	I	Vertical sync signal input, negative logic.
39	HSYNC	I	Horizontal sync signal input, negative logic.
40 41	OSC1 OSC2	I O	Sign display clock input/output. Typical 5.0 MHz. Oscillating only when sign is displayed.
42	VDD	I	Supply voltage (5.0 V) input



	Setting mode*	Search mode*	Memory mode*
	CH-CALL	COLOUR SYSTEM	MEMORY
	CH-UP	BRIGHT-UP	VOL-UP
AUDIO SYSTEM		BRIGHT-DOWN	VOL-DOWN

Key matrix *: Switch No marking: Pushbutton

5. LCD INTERFACE CIRCUIT (TR3P89)

The interface IC is dedicated to TFT colour LCD panels.

Features

This IC has the following circuits built-in.

- Gamma correction circuit
- Polarity inversion circuit for TFT LCD panels
- Common inversion circuit
- RGB 2-input switching circuit
- White balance adjustment circuit
- Sync separation circuit

Circuit behaviour

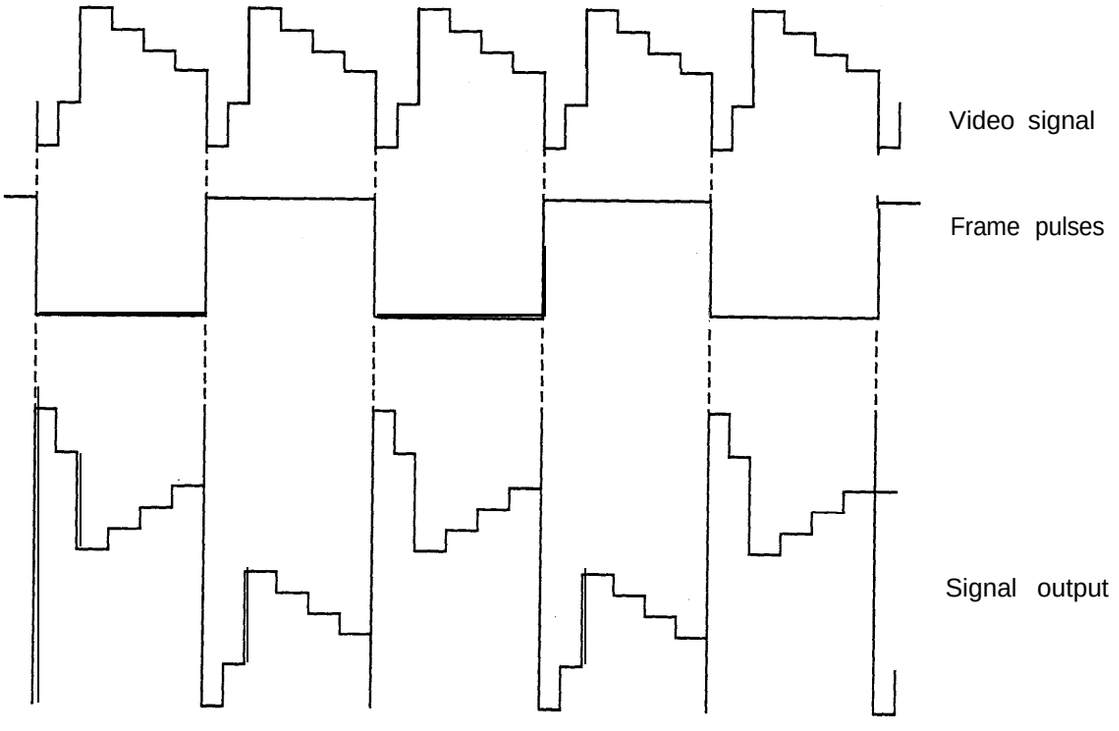
The R, G and B signals, which have been converted from the video signal by IC801 and TA8795F, are fed to pins (I), (2) and (3) respectively. These signals go through the pedestal clamp circuit first and then the white balance circuit.

White balance adjustment is made with VR810 (red sub-brightness control), VR812 (red sub-contrast control), VR806 (blue sub-contrast control) and VR807 (blue sub-brightness control).

After the white balance adjustment circuit, the signals are sent to the gamma correction circuit. In this circuit, the drive curve of the video signal is corrected according to the LCD panel's characteristics. How much to correct is determined by the voltages at pins (17) and (28).

The gamma-corrected signals proceed to the inverter stage, where the positive and negative polarities are switched over in sync with the frame pulses being applied at pin (29) from the LCD panel. The resulting signals go out of pins (22), (24) and (26) into the transistors Q861, Q862 and Q863. After being buffered in these transistors, the signals are outputted to the LCD panels.

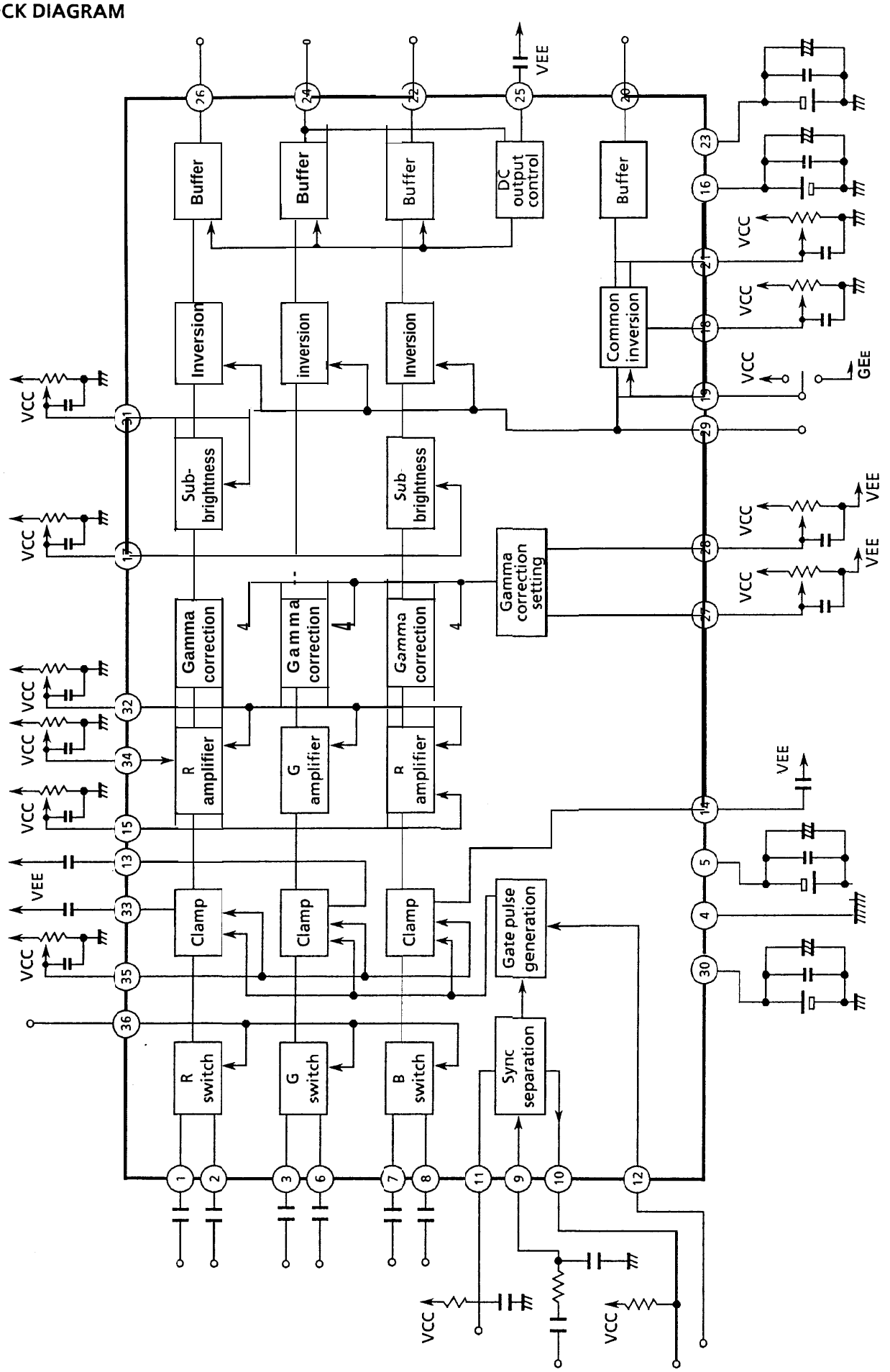
The on-screen display signal for channel signs, for example, are sent from pins (2), (3) and (4) of the microcomputer IC401 to pins (6), (7) and (8) of IC802. These signals and the video signal are switched each other by the voltage being applied at pin (36).



Pin Description

Pin No.	Name	Pin No.	Name
1	RI IN	19	COMMON INV
2	CI IN	20	COMMON OUT
3	B1 IN	21	COMMON SWING
4	GND	22	B OUT
5	VEE1	23	VEE 2
6	R2 IN	24	G OUT
7	G2 IN	25	OUT DC V DETECT
8	B2 IN	26	ROUT
9	SYNC SEP IN	27	GAMMA 1
10	SYNC OUT	28	GAMMA 2
11	TIME CONSTANT	29	INV
12	SYNC IN	30	VCC 2
13	CLAMP(G)	31	R SUB BRIGHT
14	CLAMP(B)	32	CONTRAST
15	B SUB CONTRAST	33	CLAMP (R)
16	VCC1	34	R SUB CONTRAST
17	B SUB BRIGHT	35	BRIGHT
18	COMMON DC VOLT	36	SW

BLOCK DIAGRAM



6. FLUORESCENT LAMP DRIVE CIRCUIT (DC-AC INVERTER CIRCUIT)

Since the fluorescent lamp operates on AC power, a DC-AC inverter circuit is needed to convert DC to AC when the supply power voltage is DC. A high voltage is also required to drive the fluorescent lamp. On this model, a voltage greater than 1500 Vp-p is applied across the fluorescent lamp. See the fluorescent lamp drive circuit in Fig. 6-2. The supply voltage is applied at pin (3) of the inverter transformer. The voltage at the base of Q759 remains the same; Q759 is therefore stays off, and Q760 as well as Q761 remain off too. When the power is turned on, Q759 is activated and either of Q760 or Q761 turns on earlier than the other. As a result, the circuit begins to oscillate at the resonant oscillation frequency which is determined by the capacitance (C) of C758 and the inductance (L) of the transformer's primary winding. Pins (1) and (5) of the transformer's tertiary winding are connected with the bases of Q760 and Q761 for forward feedback. Fig. 6-1 shows the relevant voltage waveforms. A vertically symmetrical sine wave is generated between pins (2) and (4) of T702. The secondary voltage between pins (6) and (9), which is proportional to the transformer's winding ratio, is given out to drive the fluorescent lamp. Once discharging has started, the fluorescent lamp's internal resistance goes down (negative resistance). By dividing the capacitance (C) of C761, a constant discharge current flows to keep the fluorescent lamp on. During arc discharge, the fluorescent lamp gives out ultraviolet rays. By means of the fluorescent substance applied over the inner surface of the glass light emitting tube, the ultraviolet rays are turned visible. This visible light is used as the backlight of the LCD panel.

- Votage waveforms

Between pin (2) of T702 and ground

Between pin (4) of T702 and ground

Between pin (2) and (4) of T702

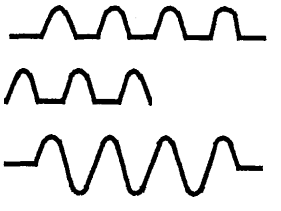


Figure. 6- 1

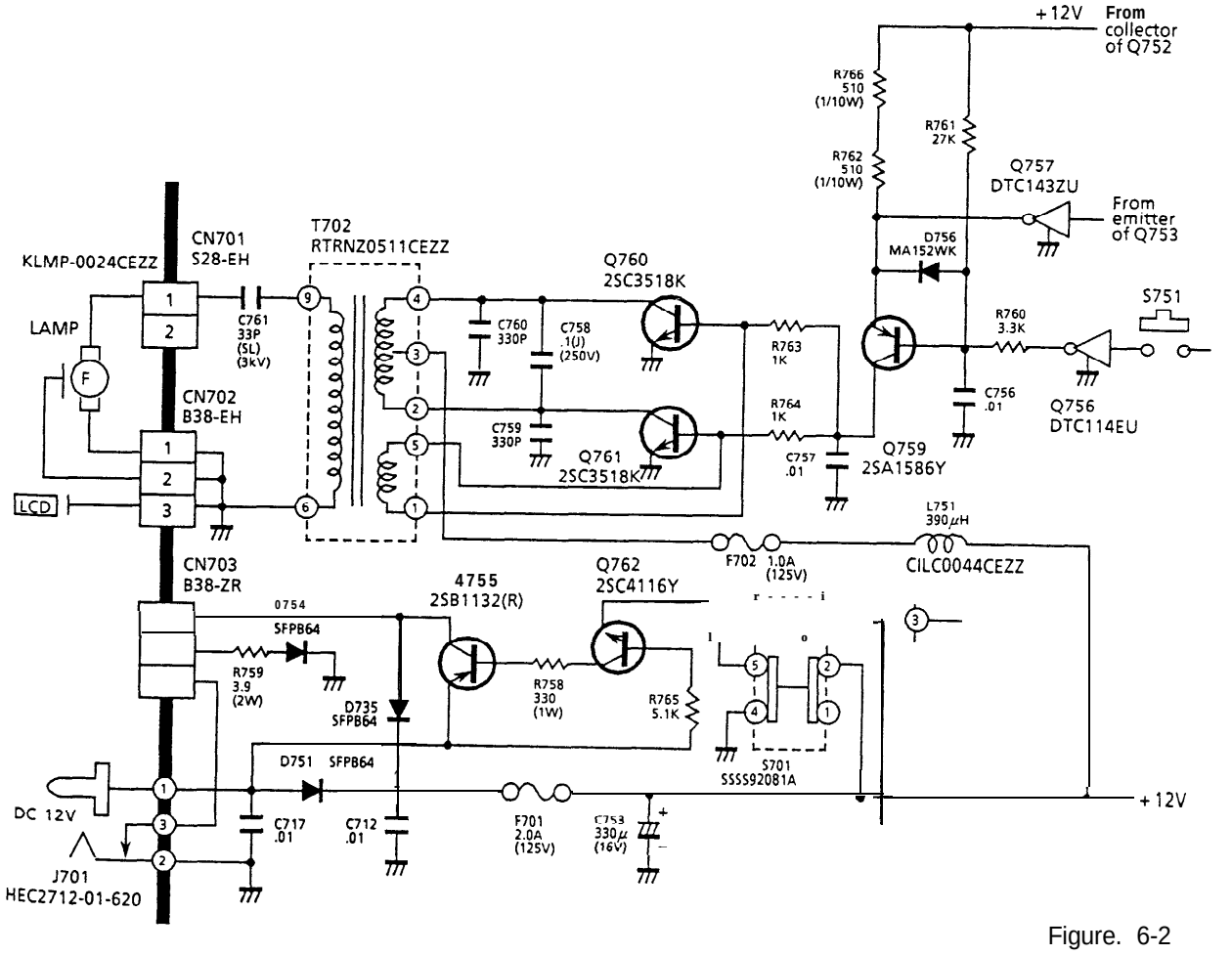
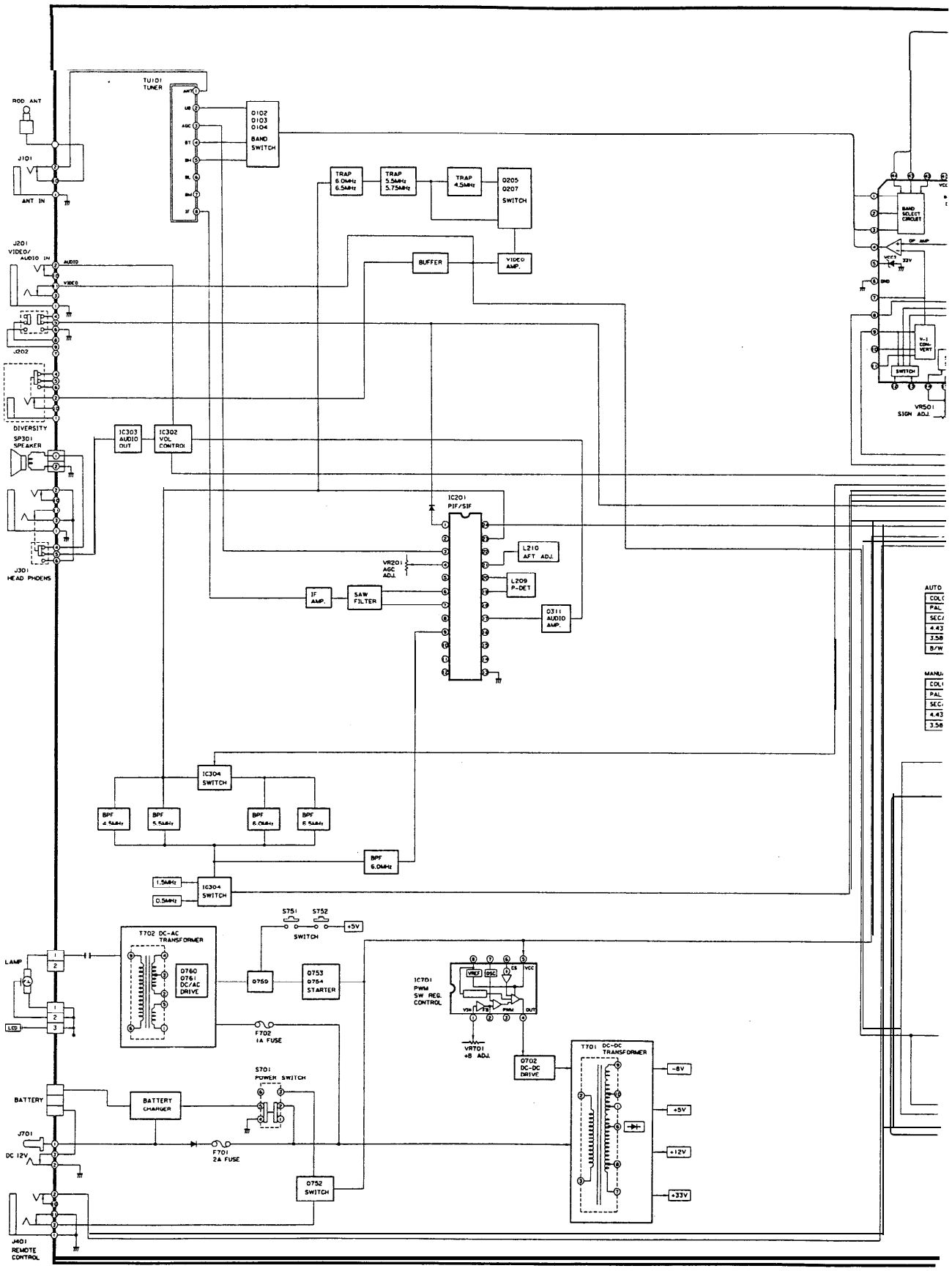
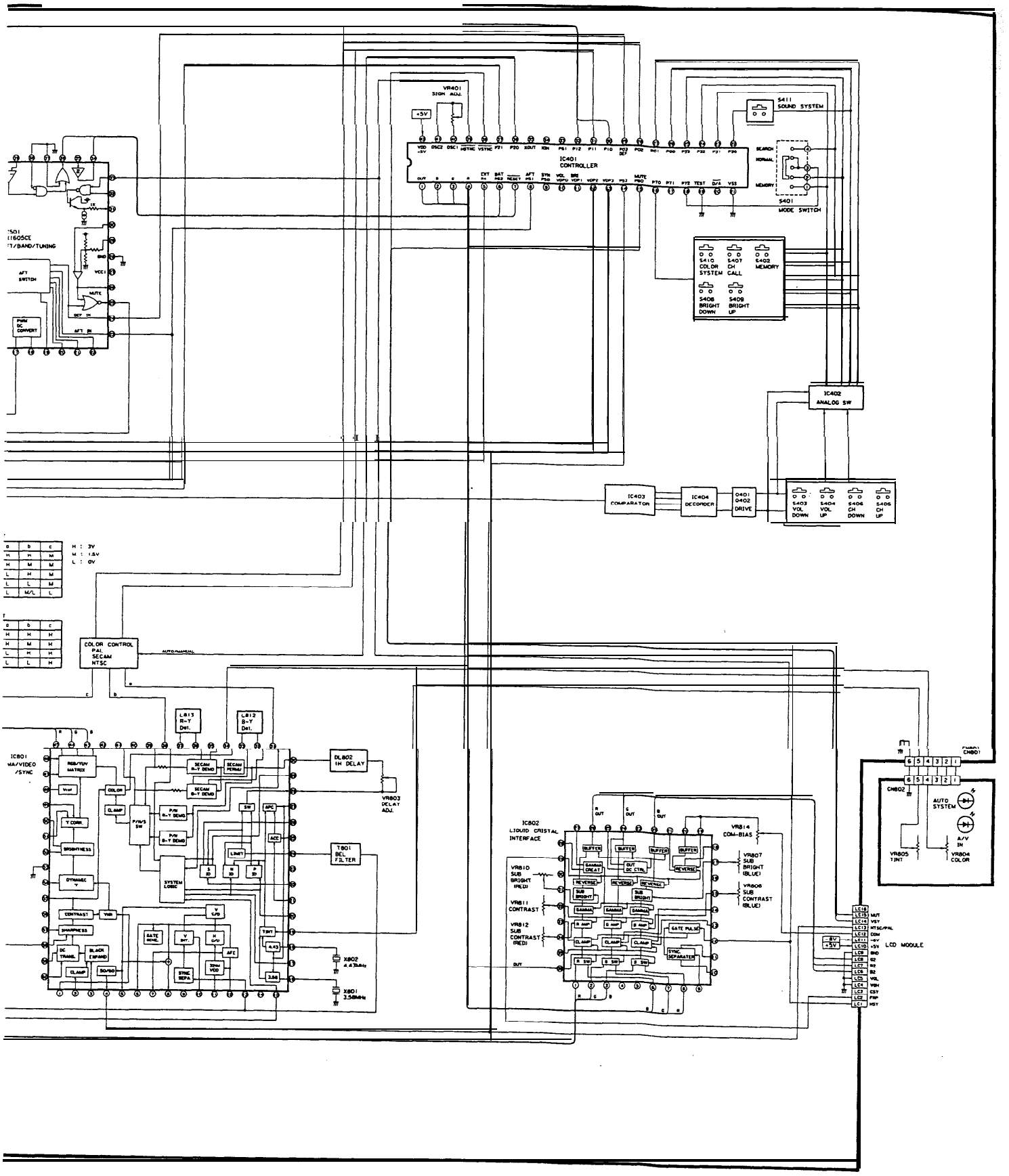


Figure. 6-2

7. BLOCK DIAGRAM

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S401
MODE SWITCH
S411
SOUND SYSTEM
IC402
ANALOG SW
IC403
COMPARATOR
IC404
DECONDER
COLOR CONTROL
PAL
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